REMARKS

This is in full and timely response to the Office Action dated September 10, 2007.

Claims 27-28, 40 and 45-52 are currently pending in this application, with claims 27, 40 and 45 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Rejection under 35 U.S.C. §112

Paragraph 3 of the Office Action indicates a rejection of claims 31 and 37-39 under 35 U.S.C. §112, second paragraph.

This rejection is traversed at least for the following reasons.

While not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, claims 31 and 37-39 have been canceled.

Withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. §103

Claims 26-44 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki)

This rejection is traversed at least for the following reasons.

Claims 26, 29-39, and 41-44 - While not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, claims 26, 29-39, and 41-44 have been canceled.

Claims 27-28 - Claim 28 is dependent upon claim 27. Claim 27 is drawn to a data processing apparatus comprising:

> a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data;
>
> a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal, said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address;
>
> a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and
>
> a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Sagane and Suzuli, either individually or as a whole, fail to disclose, teach, or suggest a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data.

Claim 40 - Claim 40 has been placed into independent form. At least for the following reasons, if the allowance of claim 40 is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested.

Claim 40 is drawn to a data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address,

wherein another program address indicates a location within said program memory for another of the instruction codes, and

wherein said value of the counter register is incremented by 1.

Sagane - Sagane ***fails*** to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein said value of the counter register is incremented by 1.

Suzuki - The Office Action cites Suzuki for the features that are deficient from within Sagane.

As shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the residual 2 bits (MSB and bit 6) are set to express the *number of correcting portions* in the module, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)) (Suzuki at column 4, lines 41-45).

As a rule, the teachings, suggestions or incentives supporting the obviousness-type rejection must be clear and particular. Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

However, Suzuki ***fails*** to disclose, teach, or suggest that number of correcting portions is *incremented by 1*. Instead, Suzuki merely teaches that the stored number of correcting portions S is ***decremented*** (step S28) (Suzuki at column 6, lines 61-62). The Office Action ***fails*** to provide any objective evidence sufficient to show that decrementing and incrementing the number of correcting portions are one in the same.

To account for these deficiencies within Suzuki, the Office Action concludes, *without providing any supporting evidence*, that a person of ordinary skill in the art at the time the invention was made *could* implement the counter register such that the value is incremented by 1 *rather than* decremented by 1 with predictable results (Office Action at page 12).

Assertions of technical facts in areas of esoteric technology ***must always be supported by citation to some reference work*** recognized as standard in the pertinent art. *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

Here, the Office Action ***fails*** to show where within Suzuki there is taught that *a specific amount* by which the stored number of correcting portions S is decremented, or that the stored number of correcting portions S is *decremented by 1*.

Moreover, the Office Action ***fails*** to show where within Suzuki there is taught that the stored number of correcting portions S *is* ***INCREMENTED*** or that the stored number of correcting portions S ***is INCREMENTED by 1***.

Nevertheless, the Office Action asserts that it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value of the counter register is ***incremented by 1*** (Office Action at page 12).

In response, incrementing is ***absent*** from within Suzuki. Instead, Suzuki arguably teaches that as a result of the ***decrement***, it is checked whether or not the number of correcting portions is 0 (Suzuki at column 6, lines 62-64).

The Office Action urges that one ***could*** implement Suzuki such that the value is initialized to 0 and step S29 (FIG. 4B) checks for whether the value is equal to the number stored in step S5 (FIG. 4A), *rather than checking for whether the value is equal to 0* (Office Action at page 12).

In response, such a retrospective view *is not a substitute* for some objective teaching or suggestion supporting an obviousness rejection since the assertions and urgings presented within the Office Action amount to nothing more than an "obvious-to-try" situation.

Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990).

Moreover, an invention is "obvious-to-try" where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful. *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious-to-try" is not the standard under §103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

- ***Thus, Sagane and Suzuli, either individually or as a whole, fail to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein said value of the counter register is incremented by 1.***

Withdrawal of this rejection and allowance of the claims is respectfully requested.

Newly added claims

Claims 45-52 - Claims 46-52 are dependent upon 45. Claim 45 is drawn to a data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

Sagane and Suzuli, either individually or as a whole, fail to disclose, teach, or suggest a central processing unit adapted to process interrupt functions of *different priority levels*, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal.

Sagane and Suzuli, either individually or as a whole, fail to disclose, teach, or suggest a counter register adapted to store a value, said value being *incremented by 1* when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address, wherein said counter register is *set to 0* during said initialization processing.

Allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: October 1, 2007

Respectfully submitted,

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